REMARKS

Applicants have canceled claims 1-6 and have added new claims 32-48. In view of the following remarks, Applicants hereby request further examination and reconsideration of the application, and allowance of claims 32-48.

The Office has rejected claims 1-6 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Office asserts that in claim 1, the phrase "wherein . . . demultiplexed" on lines 2-3 is vague because the manner in which the signals are selected and/or demultiplexed has not been clearly defined. In view of the Applicants' cancellation of claims 1-6, the Office is respectfully requested to reconsider and withdraw this rejection.

The Office has rejected claims 1-6 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,827,336 to Acampora et al. ("Acampora") or U.S. Patent No. 5,568,203 to Lee ("Lee"). The Office asserts that Acampora discloses an analog bus (the color matrix signals from the television camera, the analyzers and/or from the controller) having a plurality of parallel signal busses, wherein the signals are selected (coded, analyzed) onto the busses prior to being demultiplexed by demultiplexers (Figures 2 and 5-9). The Office also asserts that Lee discloses a system for estimating real time motion comprising at least an analog bus (from previous blocks PBs) having a plurality of parallel signal busses, wherein the signals are selected onto the busses prior to being demultiplexed by demultiplexers (110, 140).

As discussed above, claims 1-6 have been canceled and claims 32-48 have been added. Neither Acampora nor Lee, alone or in combination, anticipate, suggest, or disclose, "a plurality of first switches, each of the plurality of first switches is coupled between one of the plurality of signal streams and one of the plurality of signal buses . . . a control system coupled to each of the first plurality of switches, the control system controls when at least one of the first plurality of switches is closed to allow the signal from one of the plurality of signal streams . . . to substantially charge one of the plurality of signal buses . . . which is not currently being read at the output." as recited in claim 32 or "allowing at least another one of the signals to substantially charge at least another one of the plurality of signal

buses that is not being read at the output while the one of the signals is being read . . . reading the at least another one of the signals at the output after the at least another one of the plurality of signal buses is substantially charged with the another one of the signals" as recited in claim 41.

The Office's attention is respectfully directed to col. 7, lines 12-16 and to FIGS. 2 and 5-9 in Acampora which illustrate and state that DPCM signals are input for a time division multiplexer 60 which interleaves them on per scan line basis to supply a continuous sample stream as an input signal for code assembler 62. Accordingly, Acampora only discloses interleaving data on to one bus. Nowhere does Acampora teach or suggest multiple buses on which the signals are transferred, let alone multiple buses where one of the buses which is not being read by the output is charged with one of the signals while another one of the plurality of signal buses has its signal read at the output. Additionally, Acampora does not teach or suggest a first plurality of switches coupled between one of the plurality of signal streams and one of the plurality of signal buses and/or a control system coupled to each of the first plurality of switches to control the operation of the switches to allow the signals to substantially charge the buses.

The Office's attention is also respectfully directed to col. 4, lines 37-40 and FIG. 3 in Lee which state and illustrate that, "First demultiplexor 110 sequentially receives the pixel data string of upper sixteen rows of the search window for each column and demultiplexes the received pixel data strings to be supplied on a row by row basis to first latch 120." Accordingly, Lee discloses demultiplexing the pixel data on to rows, but does not allowing one of the signals to charge one of the plurality signal buses which is not currently being read while a signal on another one of the plurality of signal buses is read. Lee also does not disclose a control system that controls switches to allow the signal from a signal stream to substantially charge one of a plurality of signal buses which is not currently being read at the output while another signal on another signal bus is being read at the output.

As discussed at page 10, lines 15-29 of the above-identified patent application with reference to one illustrative embodiment, "The purpose of selecting the current column and preselecting the next three columns is to allow the video bus to charge up to the proper value and settle prior to being demultiplexed as shown in Figure 7 circuit 24. By pre-

selecting the three columns (or pixel time constants) ahead of time, the column video processing circuitry only has to drive the video bus at one quarter the actual read rate (one-fourth the bandwidth) and therefore can be made smaller and lower power than they otherwise would have to be. Also since each column is connected to only one out of every four columns the video bus has only one fourth of the capacitance, because there are only one fourth of the transmission gates (or switches) to drive . . . The analog pre-charging is done at one-fourth the bandwidth in Figure 7 than the prior art conventional single ended video bus and only the demultiplexing is done at the normal bandwidth." As a result, the present invention provides a number of advantages, including providing lower power, capacitance and bandwidth requirements. Accordingly, in view of the foregoing remarks, claims 32 and 41 are believed to be distinguishable over the cited references and patentable. Since claims 33-40 depend from and contain the limitations of claim 32 and claims 42-48 depend from and contain the limitations of claim 41, they are distinguishable over the cited references and are patentable in the same manner as claims 32 and 41.

In view of the above, reconsideration of the outstanding Office action is respectfully requested. Pursuant to 37 CFR § 1.121, attached as Appendix A is a Version With Markings to Show Changes Made.

In view of all of the foregoing, Applicant submits that this case is in condition for allowance, and such allowance is earnestly solicited.

Respectfully submitted,

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11/20/01 (Date) | Sherri A. Moscato (Sherri A. Moscato)

Appendix A

Version With Markings to Show Changes Made

In The Claims

Please cancel claims 1-6 and add new claims 32-48 as follows:

--32. A bus system for transferring signals from a plurality of signal streams to an output, the bus system comprising:

a plurality of signal buses in parallel, each of the plurality of signal buses is coupled to the output;

a plurality of first switches, each of the plurality of first switches is coupled between one of the plurality of signal streams and one of the plurality of signal buses; and

a control system coupled to each of the first plurality of switches, the control system controls when at least one of the first plurality of switches is closed to allow the signal from one of the plurality of signal streams coupled to the closed one of the first plurality of switches to substantially charge one of the plurality of signal buses which is also coupled to the closed one of the first plurality of switches and which is not currently being read at the output.--

--33. The bus system as set forth in claim 32 wherein the control system controls when at least another one of the first plurality of switches is closed to allow the signal from another one of the plurality of signal streams coupled to the closed another one of the first plurality of switches to be read at the output from another one of the plurality of signal buses which is also coupled to the closed another one of the first plurality of switches.--

--34. The bus system as set forth in claim 32 further comprising a plurality of second switches, each of the plurality of second switches is coupled between one of the plurality of signal buses and the output, the control system controls when each of the of the plurality of second switches is closed to allow the signal on one or more of the plurality of signal buses to be read at the output.--

--35. The bus system as set forth in claim 32 wherein the control system provides binning by coupling the signals from two or more of the plurality of signals buses to be read at the output at substantially the same time to average the signals together.--

--36. The bus system as set forth in claim 32 wherein a pair of the plurality of signal buses are coupled to each of the plurality of signal streams for differential processing.--

--37. The bus system as set forth in claim 32 wherein the control system further comprises:

a decoder; and

a first control circuit coupled between the decoder and each of the first plurality of switches.--

--38. The bus system as set forth in claim 37 wherein the decoder is a sequential decoder.--

--39. The bus system as set forth in claim 37 wherein the decoder is a random decoder.--

--40. The bus system as set forth in claim 37 wherein the control system further comprises:

an address counter coupled to the decoder; and

a second control circuit coupled between the address counter and each of the second plurality of switches.--

--41. A method for transferring signals from a plurality of signal streams to an output, the method comprising:

reading at least one of the signals at an output from at least one of a plurality of signal buses, each of the plurality of signal buses is coupled to the output;

allowing at least another one of the signals to substantially charge at least another one of the plurality of signal buses that is not being read at the output while the one of the signals is being read; and

reading the at least another one of the signals at the output after the at least another one of the plurality of signal buses is substantially charged with the another one of the signals.--

--42. The method as set forth in claim 41 further comprising controlling when each of the plurality of signal buses is charged with one of the signals.--

--43. The method as set forth in claim 41 further comprising controlling when the reading at the output from each of the plurality of signal buses occurs.--

--44. The method as set forth in claim 41 wherein the reading at least one of the signals comprises binning the signals from two or more of the plurality of signals buses together to be read at the output at substantially the same time to average the signals together.--

--45. The method as set forth in claim 41 wherein the reading further comprises differential processing of the signals read from a pair of the plurality of signal buses, wherein each of the pair of the plurality of signal buses are coupled to one of the plurality of signal streams.--

--46. The method as set forth in claim 41 wherein the allowing at least another one of the signals to substantially charge at least another one of the plurality of signal buses comprises charging each of the plurality of signal buses with one of the signals in a sequential order.--

--47. The method as set forth in claim 41 wherein the allowing at least another one of the signals to substantially charge at least another one of the plurality of signal buses comprises charging each of the plurality of signal buses with one of the signals in a random order.--

--48. The method as set forth in claim 41 wherein the allowing at least another one of the signals to substantially charge at least another one of the plurality of signal

buses comprises charging each of the plurality of signal buses with one of the signals at substantially the same time.--